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(54) **MOLDED LEADFRAME SUBSTRATE SEMICONDUCTOR PACKAGE**

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Related U.S. Application Data

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(51) **Int. Cl.**
H01L 21/00 (2006.01)
H01L 23/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 21/00*** (2013.01); *H01L 23/00* (2013.01); *H01L 24/00* (2013.01); *H01L 2924/1511* (2013.01); *H01L 2924/1711* (2013.01)

(58) **Field of Classification Search**
CPC H01L 21/00; H01L 23/00
USPC 438/106; 257/690, 666–677; 29/827, 29/856, 858, 861
See application file for complete search history.

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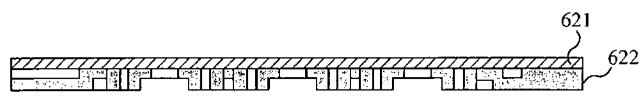
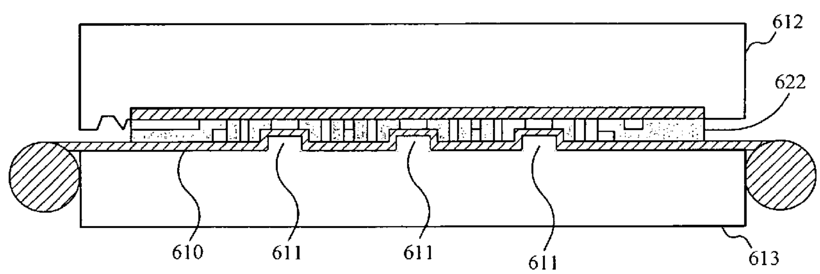
(57) **ABSTRACT**

A process for forming land grid array semiconductor packages includes a leadframe that is supported by a substrate comprising mold compound. In some embodiments, at least one die is electrically coupled to the leadframe by bondwires. The package comprises a second mold compound to act as an encapsulant. An apparatus for forming a land grid array semiconductor package includes means for molding a leadframe, assembling thereon at least one semiconductor device, applying a second mold, and singulating to form individual devices. A land grid array package comprises a leadframe, a substrate for supporting the leadframe, at least one semiconductor device and a mold compound.

17 Claims, 15 Drawing Sheets





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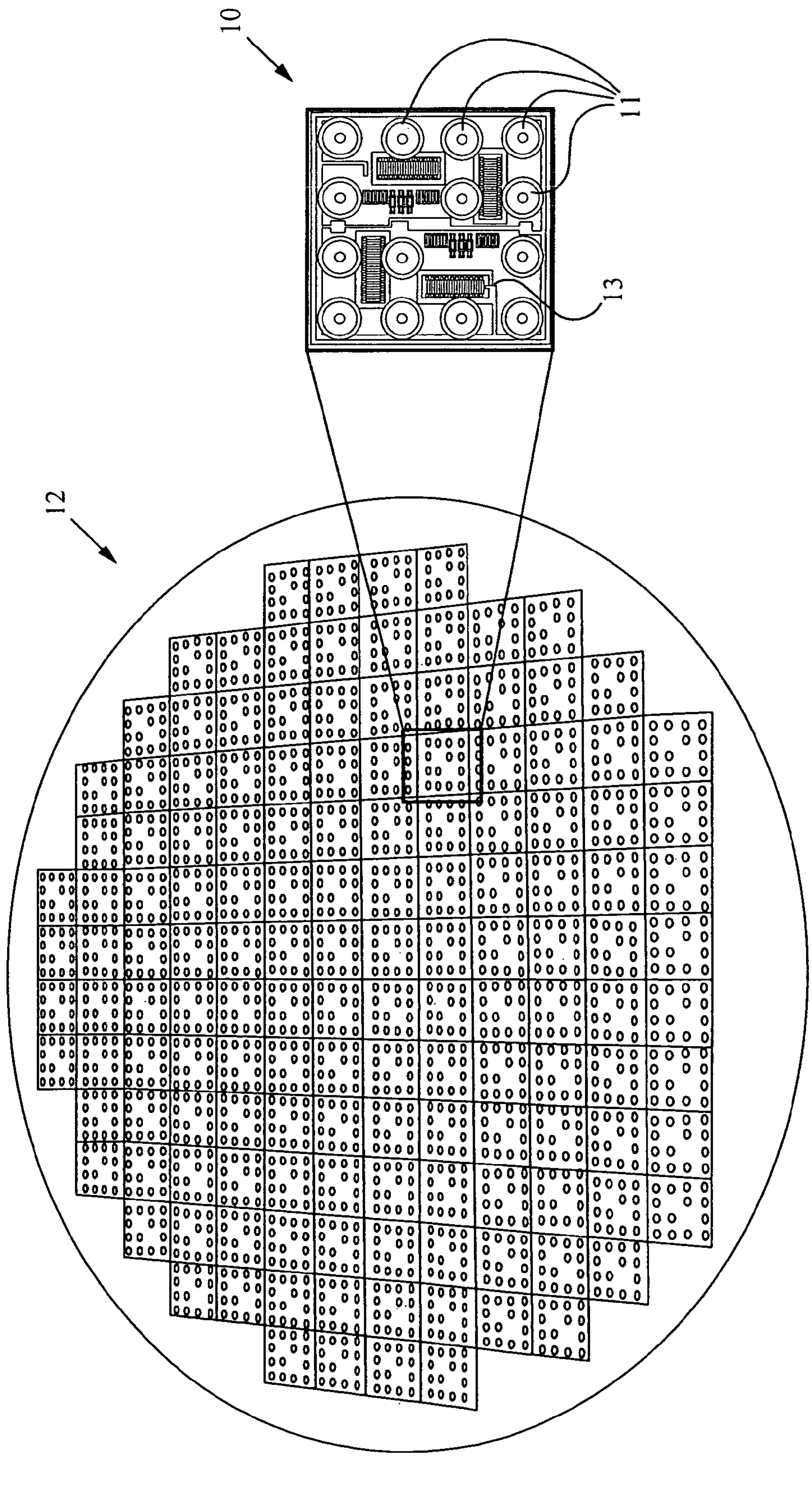

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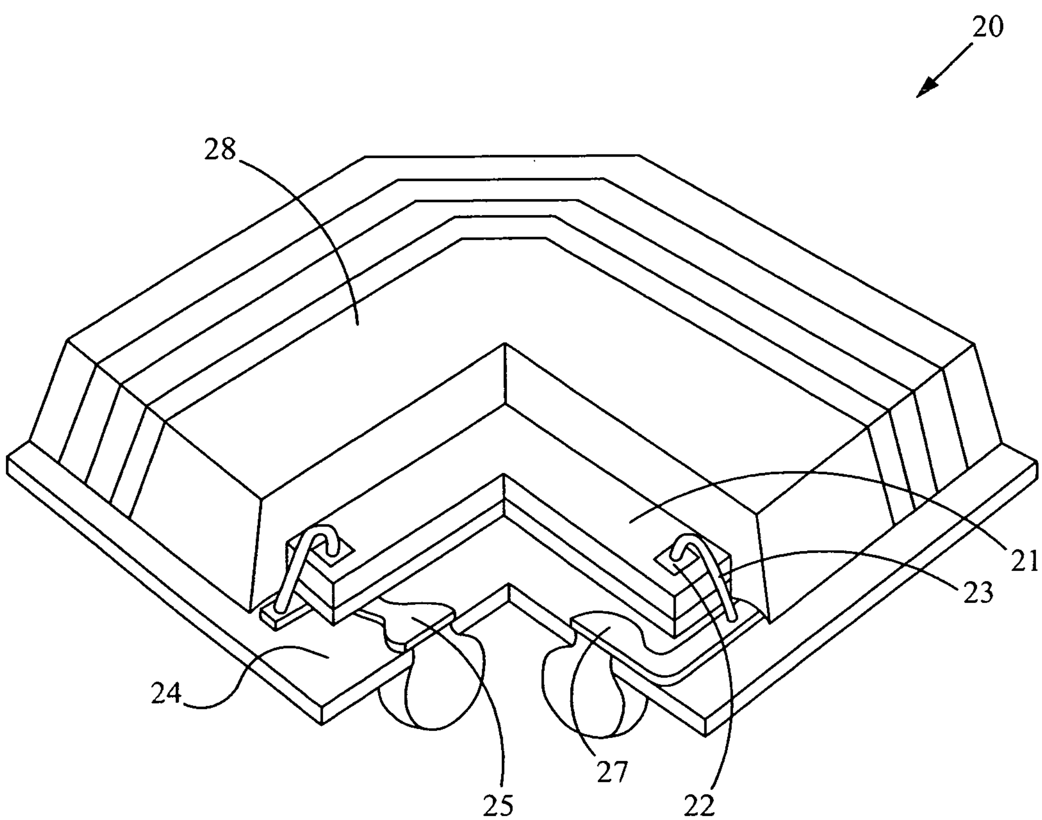

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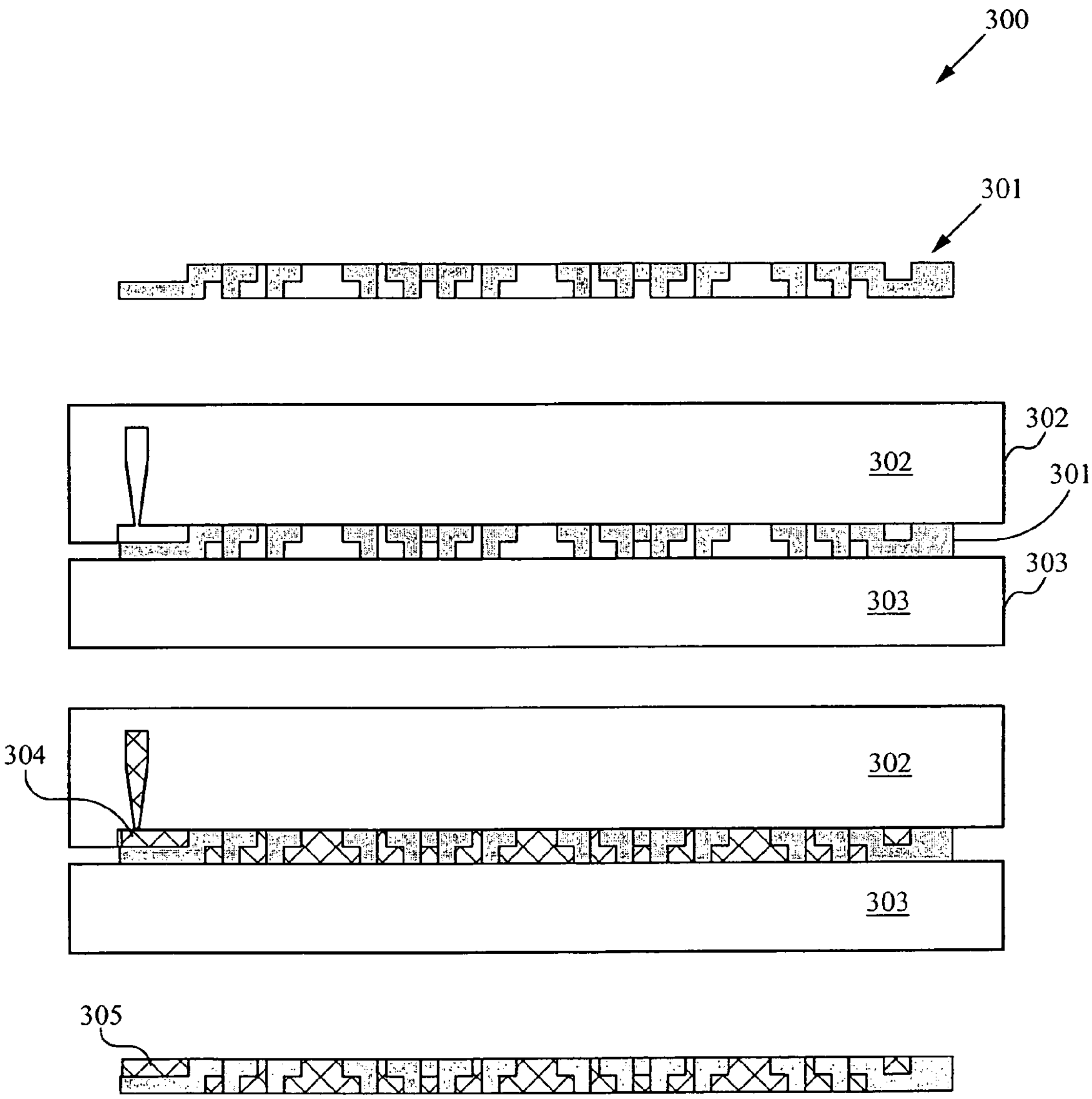
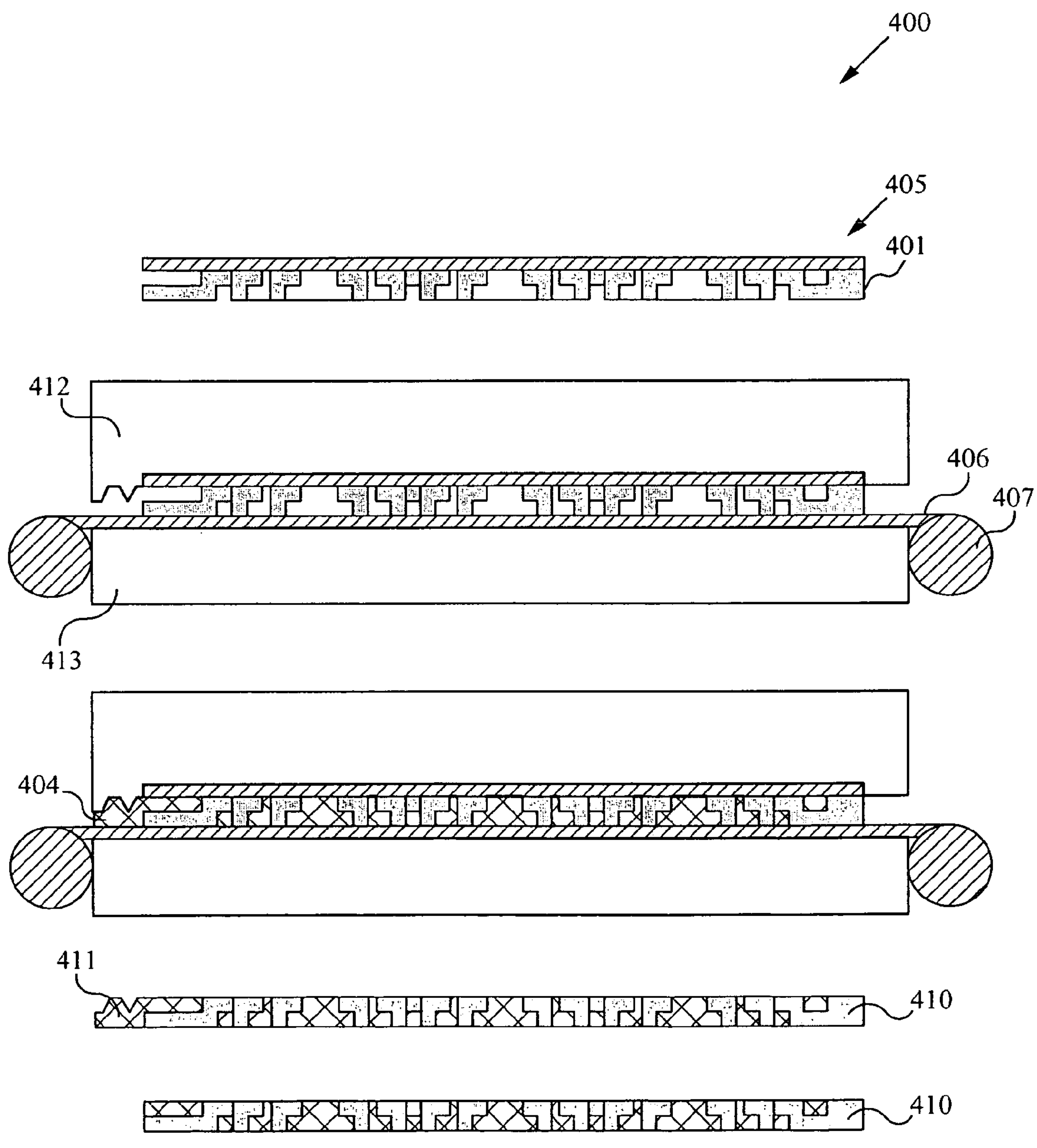


Fig. 3



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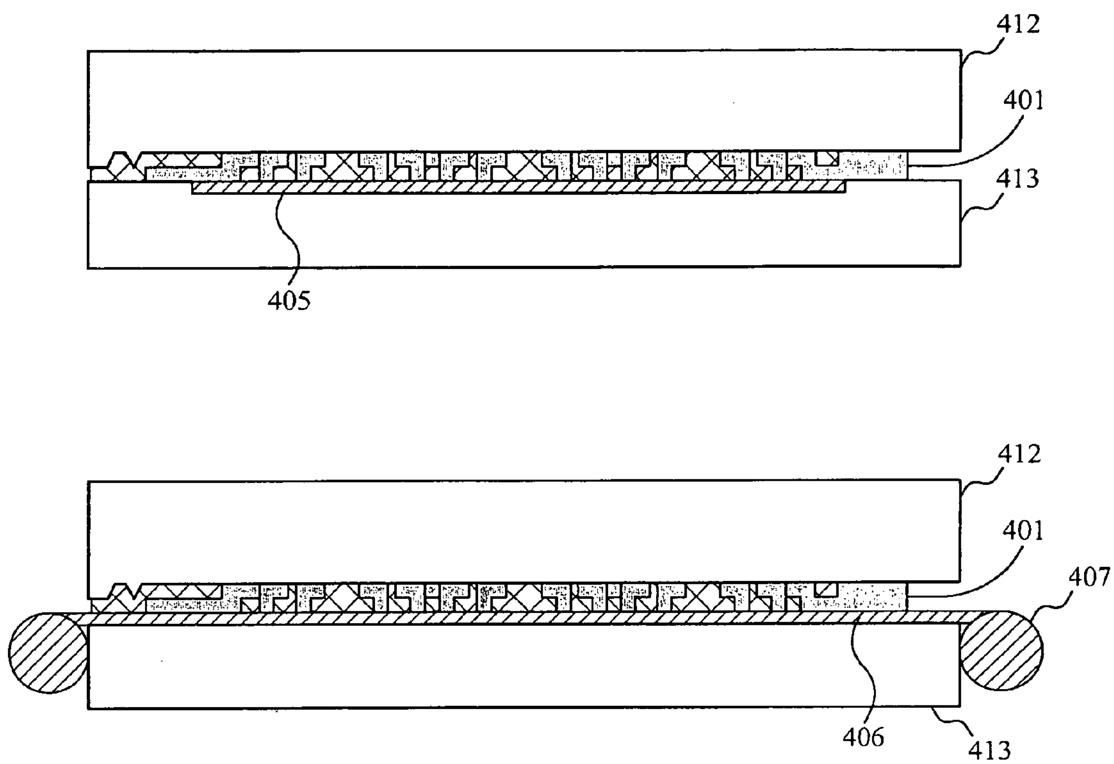

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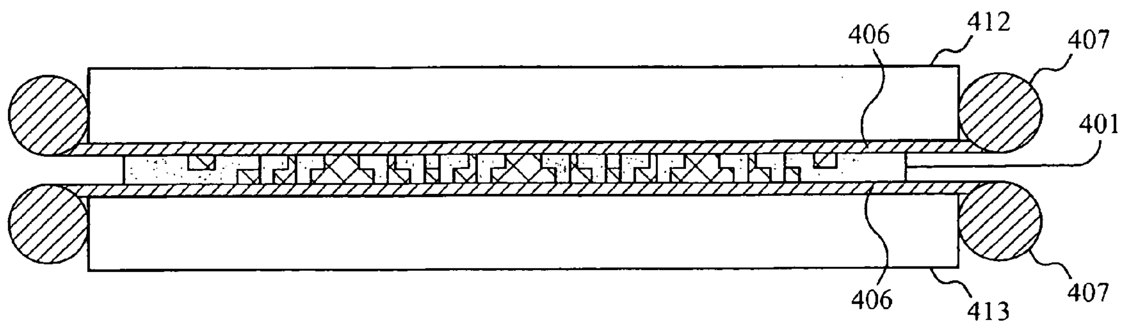

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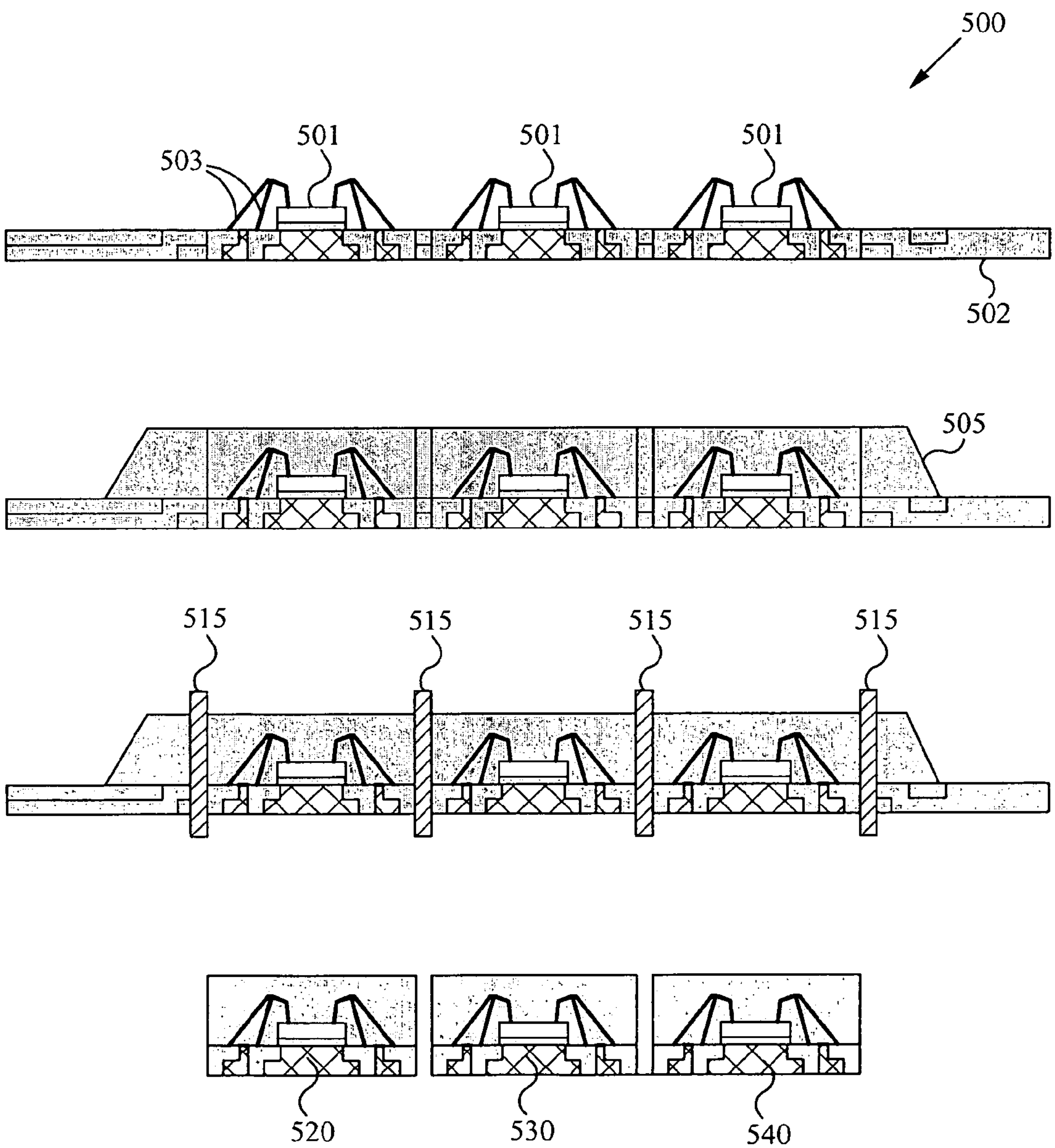

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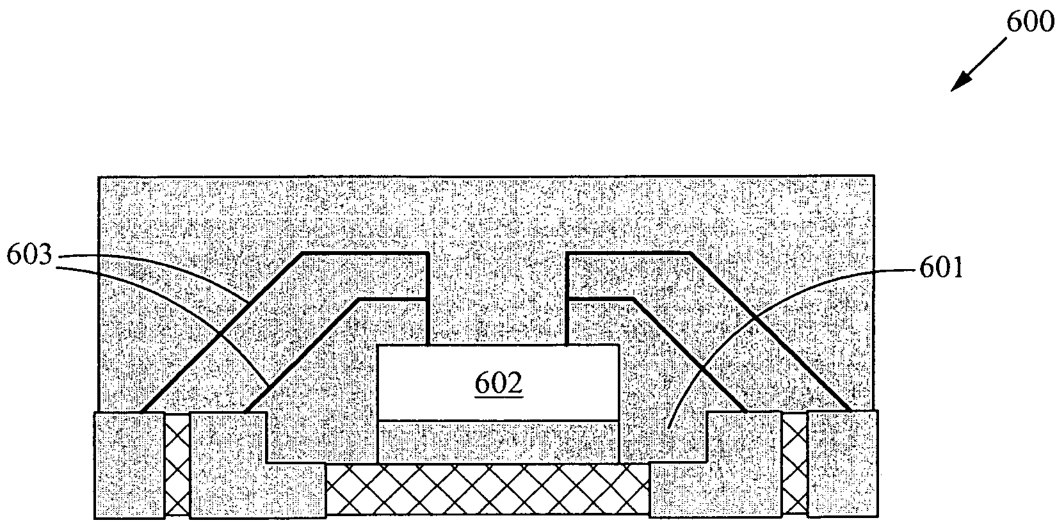

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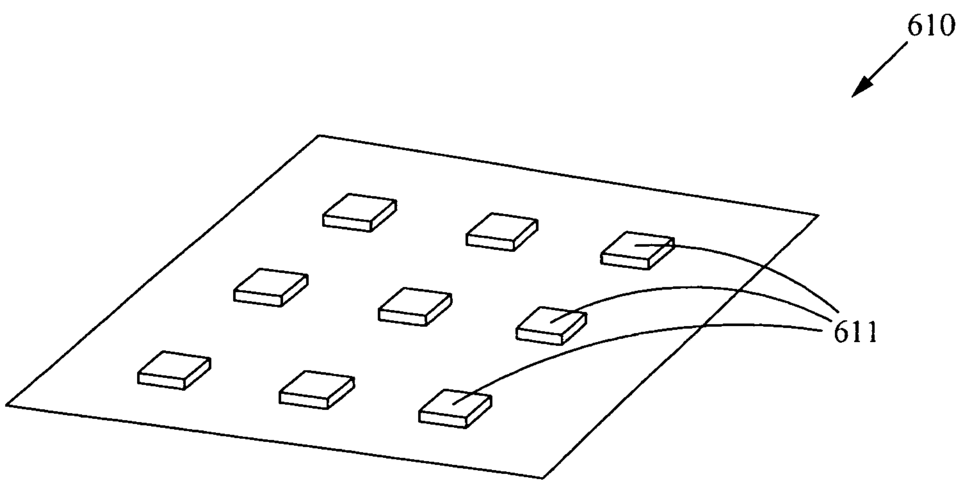

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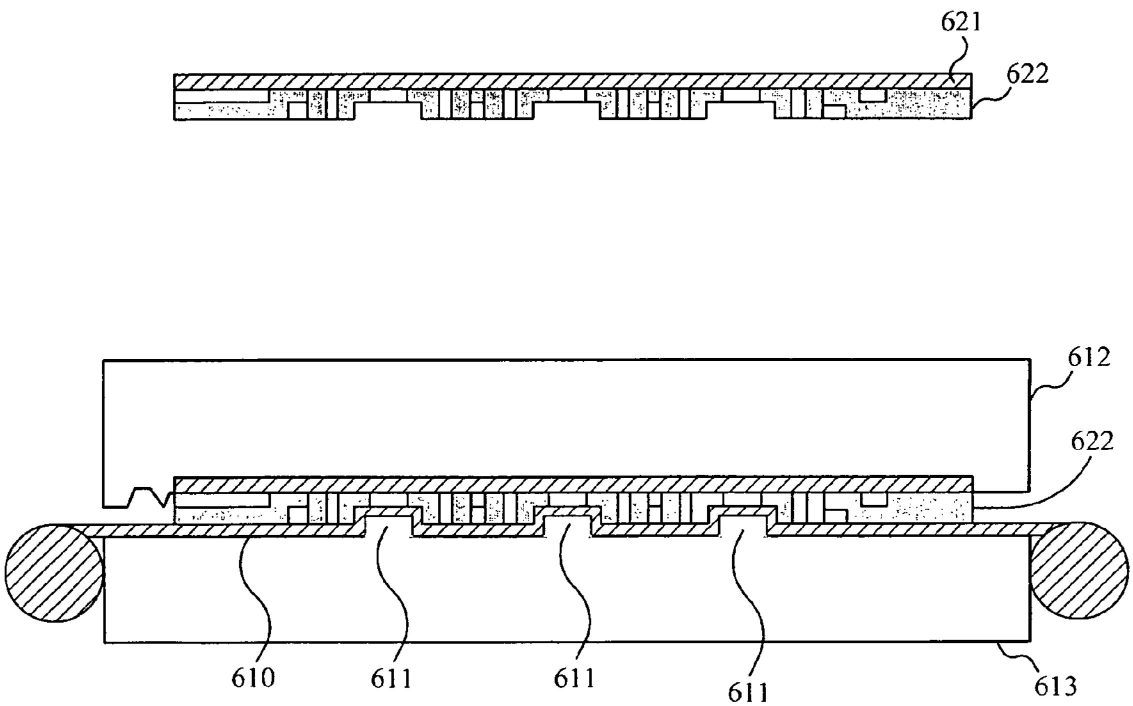

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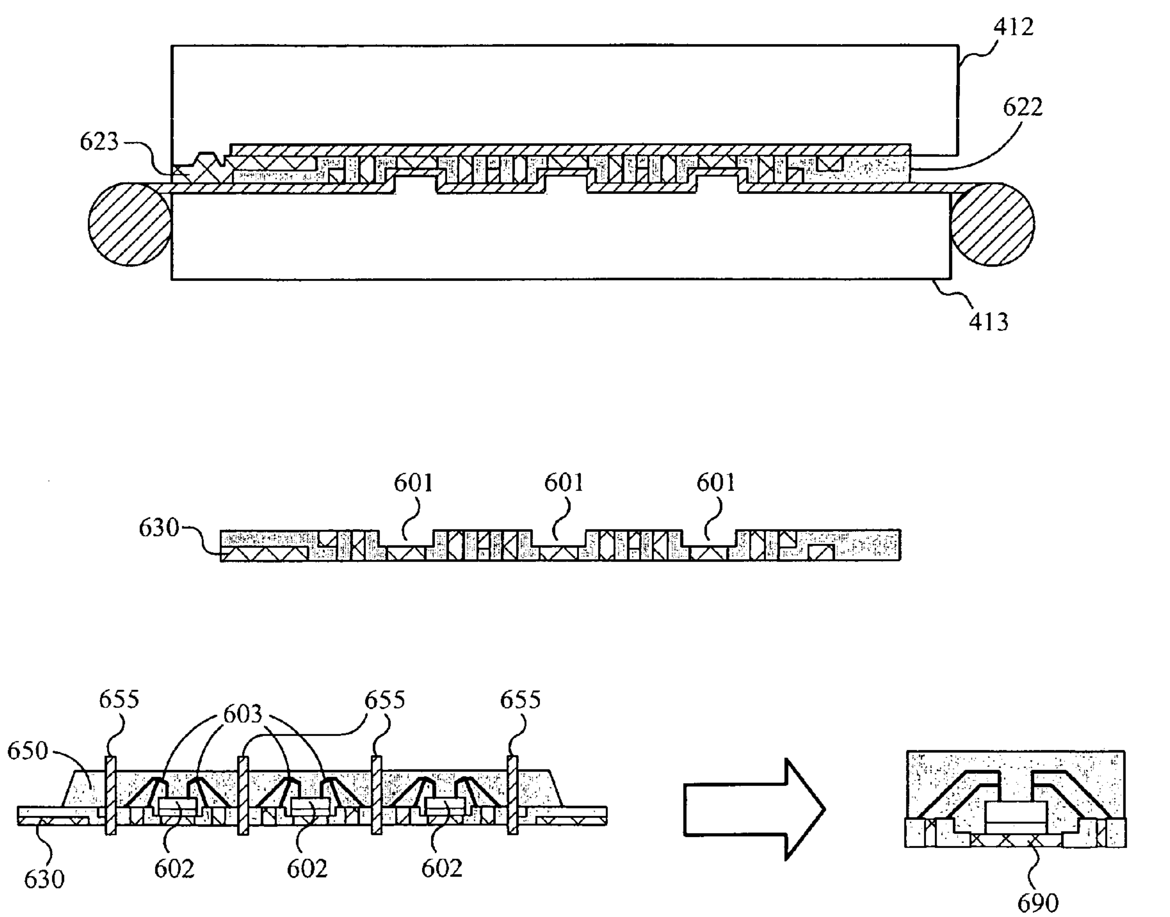
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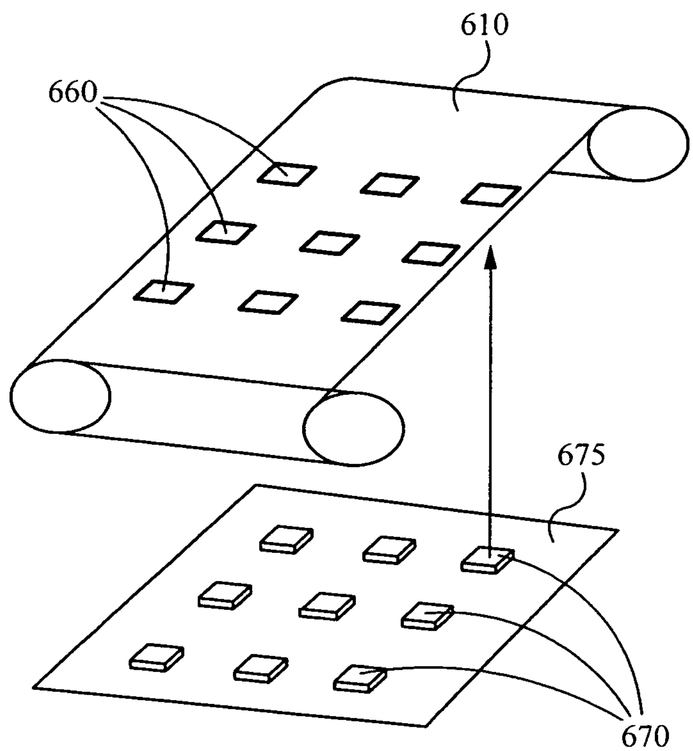
Fig. 6D



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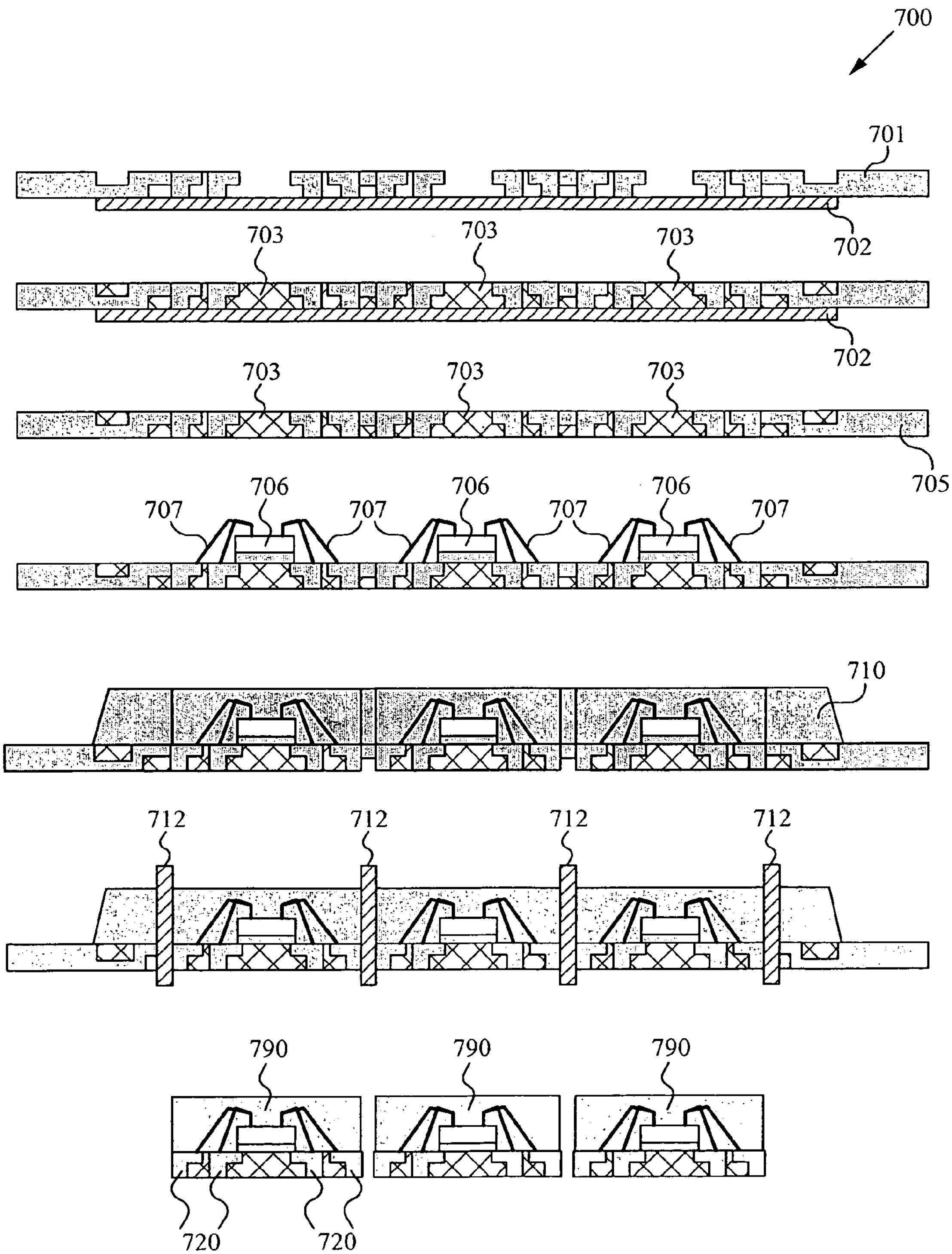
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Fig. 7

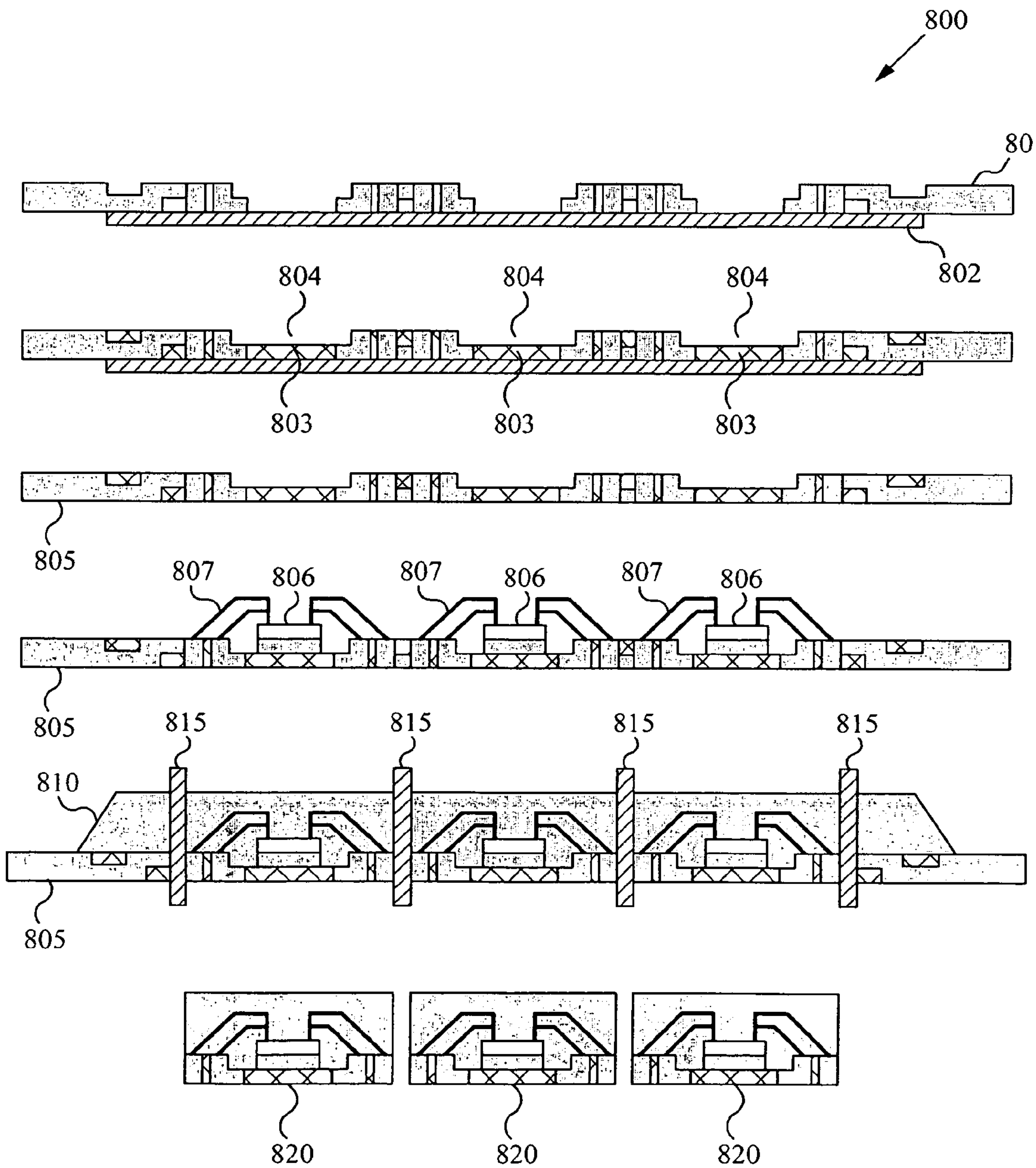
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Fig. 8

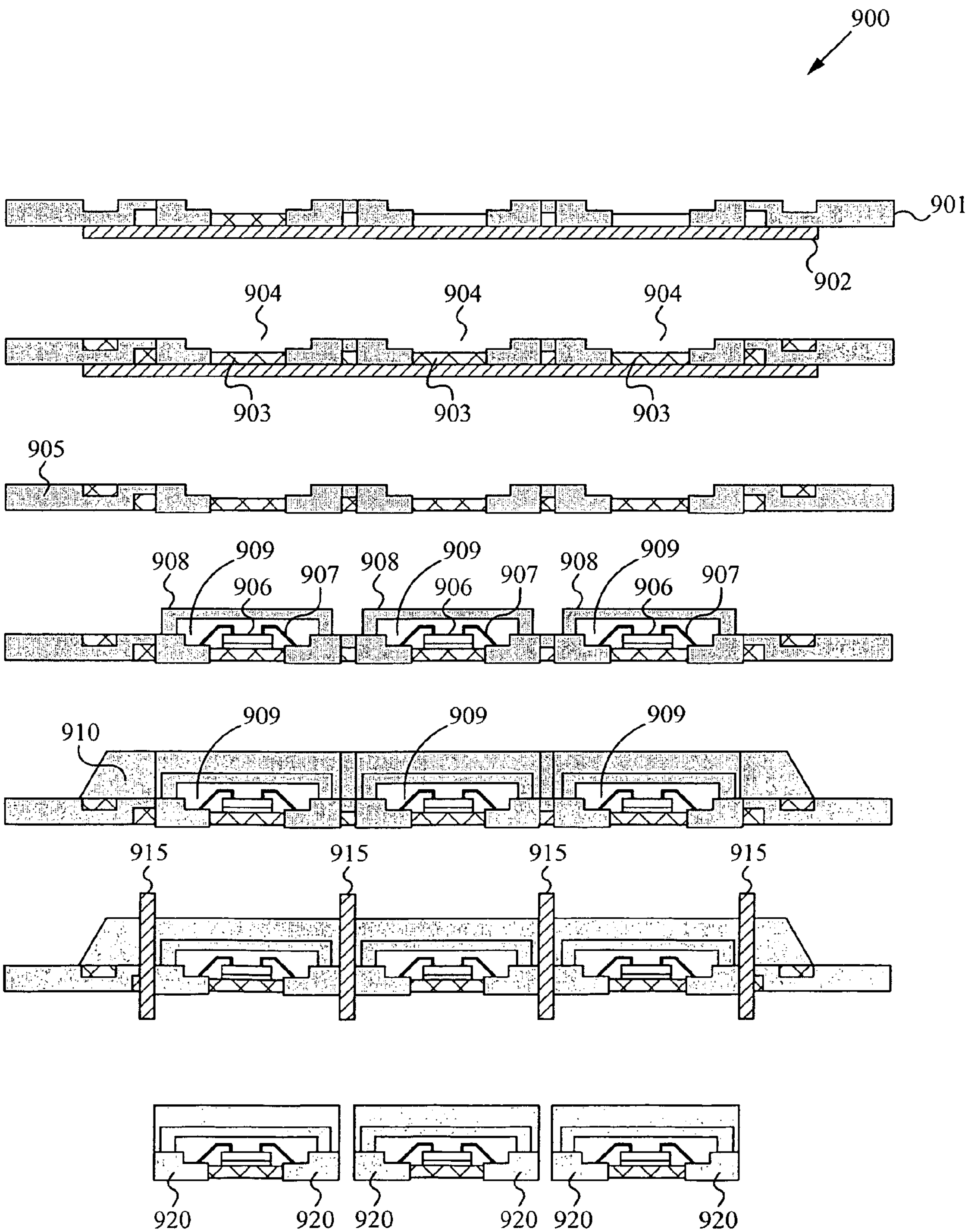
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Fig. 9

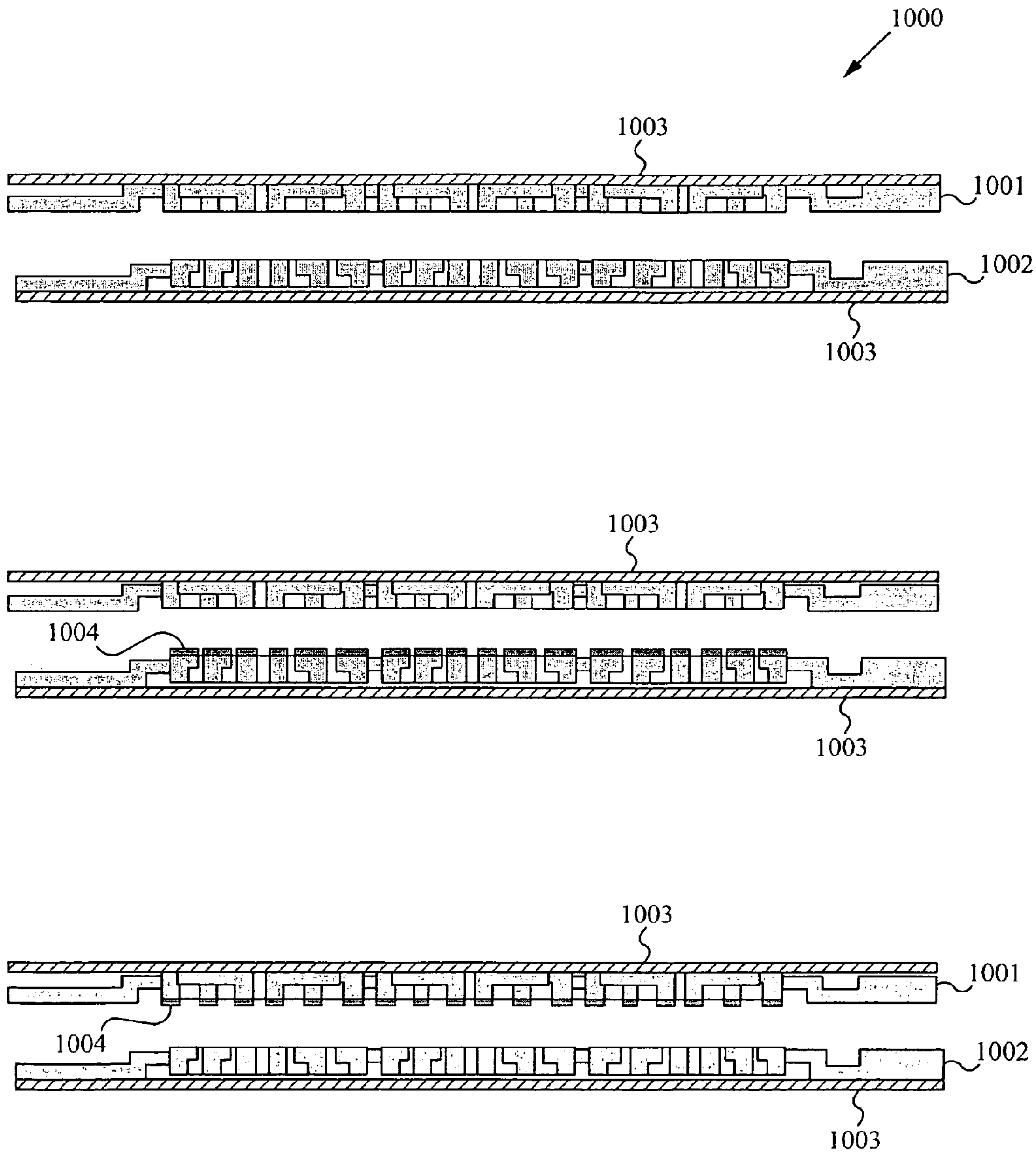
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Fig. 10A

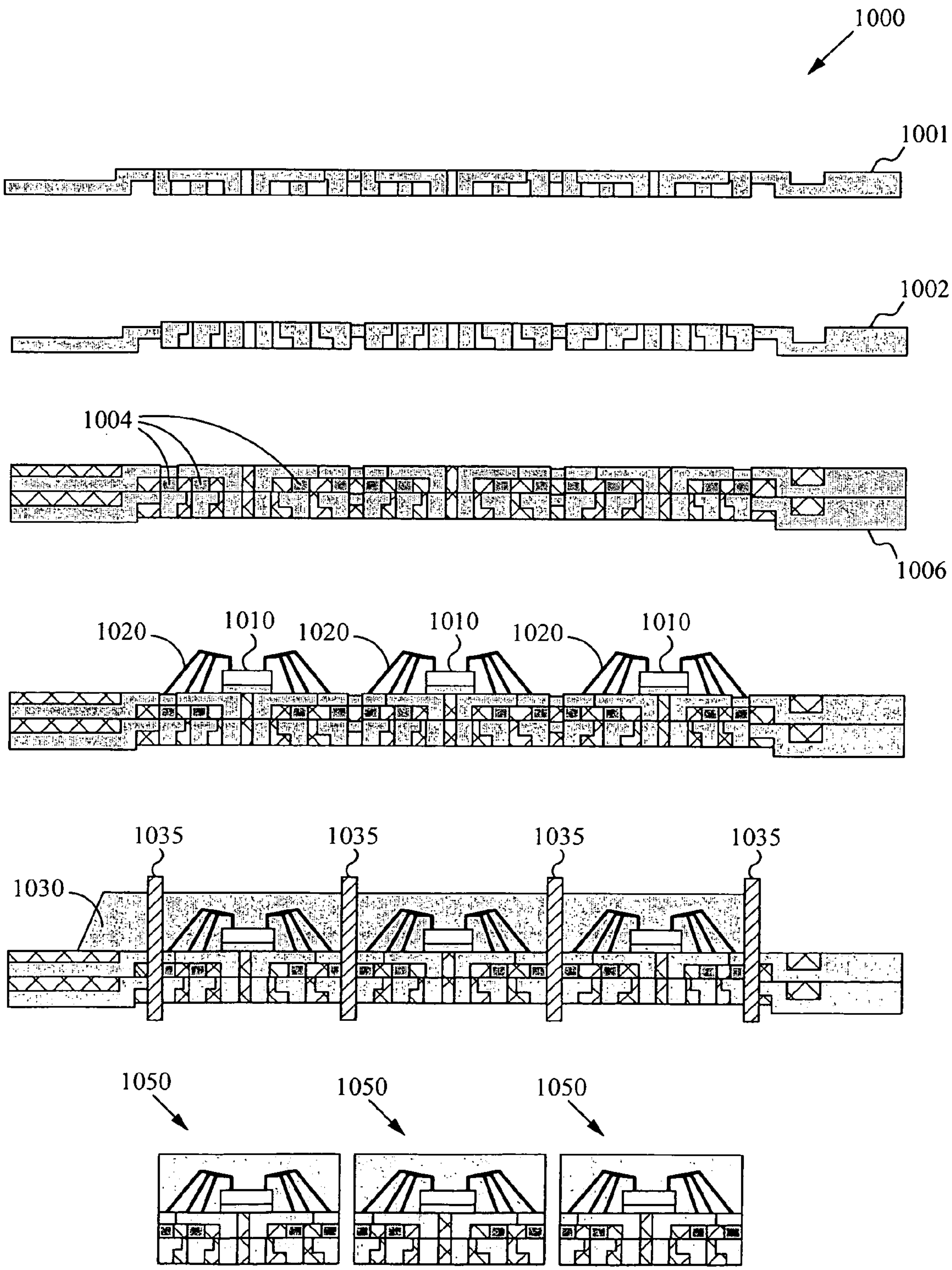
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Fig. 10B

MOLDED LEADFRAME SUBSTRATE SEMICONDUCTOR PACKAGE

RELATED APPLICATIONS

This patent application is a Divisional application which claims priority under 35 U.S.C. section 121 of the co-pending U.S. patent application Ser. No. 12/002,054, filed Dec. 14, 2007, entitled MOLDED LEADFRAME SUBSTRATE SEMICONDUCTOR PACKAGE which claims benefit of priority under 35 U.S.C. section 119(e) of U.S. Provisional Patent Application 60/875,162 filed Dec. 14, 2006, entitled MOLDED-LEADFRAME SUBSTRATE SEMICONDUCTOR PACKAGE and U.S. Provisional Patent Application 60/877,274 filed Dec. 26, 2006, entitled MOLDED-LEADFRAME SUBSTRATE SEMICONDUCTOR PACKAGE, which are all incorporated herein by reference.

FIELD OF THE INVENTION

The present invention is in the field of semiconductor packaging and is more specifically directed to package with heat transfer.

BACKGROUND

The increasing demand for computer performance has led to higher chip internal clock frequencies and parallelism, and has increased the need for higher bandwidth and lower latencies. Processor frequencies are predicted to reach 29 GHz by 2018, and off-chip signaling interface speeds are expected to exceed 56 Gb/s. Optimization of bandwidth, power, pin count, or number of wires and cost are the goals for high-speed interconnect design. The electrical performance of interconnects is restricted by noise and timing limitations of the silicon, package, board and cable. To that end, semiconductor packages must be made smaller, conforming more and more closely to the size of the die encapsulated within. However, as the size of the package shrinks to the size of the die itself, the size of the package becomes insufficient to support the number of leads generally required by current applications.

Chip Scale Packages (CSP) have emerged as the dominant package for such applications. FIG. **1** shows an example of a CSP in current practice. More specifically, the package in FIG. **1** is a Wafer Level Chip Scale Package **10** (WLCSP), commonly marketed by companies such as National Semiconductor Corporation as the Micro SMD and Maxim Integrated Products as the UCSP. Generally, solder bumps **11** are formed on processed and completed semiconductor wafers **12** before the wafers are sawn to form an individual semiconductor device **13**. Although this has dramatically reduced package size and can be useful in some instances, it suffers from drawbacks which remove it from consideration for certain applications. First, the pitch between the solder bumps **11** must be made wide enough to effectuate assembly of the device onto a printed circuit board in application. This requirement can force manufacturers to artificially grow die sizes to meet the minimum pitch, thereby increasing cost. Second, the total I/O count of the device is generally constrained due to the decreased reliability at the high bump counts. At bump counts higher than 49, or a 7×7 array, reliability becomes critical and applications such as hand held devices, which require a high degree of reliability, no long become a possible marketplace.

To overcome the issues mentioned above, the semiconductor industry has moved toward Ball Grid Array (BGA) packages. The BGA is descended from the pin grid array (PGA), which is a package with one face covered (or partly covered) with pins in a grid pattern. These pins are used to conduct electrical signals from the integrated circuit (IC) to the printed circuit board (PCB) it is placed on. In a BGA, the pins are replaced by balls of solder stuck to the bottom of the package. The device is placed on a PCB that carries copper pads in a pattern that matches the solder balls. The assembly is then heated, either in a reflow oven or by an infrared heater, causing the solder balls to melt. Surface tension causes the molten solder to hold the package in alignment with the circuit board, at the correct separation distance, while the solder cools and solidifies. The BGA is a solution to the problem of producing a miniature package for an IC with many hundreds of I/O. As pin grid arrays and dual-in-line (DIP) surface mount (SOIC) packages are produced with more and more pins, and with decreasing spacing between the pins, difficulties arose in the soldering process. As package pins got closer together, the danger of accidentally bridging adjacent pins with solder grew. BGAs do not have this problem, because the solder is factory-applied to the package in exactly the right amount. Alternatively, solder balls can be replaced by solder landing pads, forming a Land Grid Array (LGA) package.

FIG. **2** shows a cutaway image of a generic BGA package **20**. Generally, an IC **21** has bondpads **22** to which bondwires **23** are affixed. The IC **21** is mounted on a substrate **24**. In current practice, the substrate **24** is a laminate, such as polyimide. Generally, the substrate **24** is of a similar construction to a PCB. The substrate **24** has copper patterns **25** formed thereon. The bondwires **23** effectuate electrical contact between the IC **21** and the copper patterns **25**. The copper patterns **25** are electrically connected to solder balls **26** through via holes **27** in the substrate **24**. In most embodiments of BGA packages, the IC **21** is encapsulated by a mold compound **28**. Although BGA packages effectuate large I/O count devices in small areas, they are susceptible to moisture. Generally, moisture seeps into packages while awaiting assembly into a finished product, such as a computer. When the package is heated to solder the device into its end application, moisture trapped within the device turns into vapor and cannot escape quickly enough, causing the package to burst open. This phenomenon is known as the "popcorn" effect. What is needed is a semiconductor package that is robust to both structural stressors and moisture.

SUMMARY OF THE DISCLOSURE

In one aspect of the invention, a process for forming a land grid array package comprises at least partially encasing a first leadframe strip in a first mold compound thereby forming a molded leadframe strip, mounting at least one semiconductor device on the molded leadframe strip, mounting bondwires on the at least one semiconductor device to effectuate electrical contact between the semiconductor device and the molded leadframe, at least partially encasing the molded leadframe strip, the semiconductor device, and bondwires, and singulating the molded leadframe strip to form discrete land grid array packages. In some embodiments, The process further comprises embossing at least one step cavity into the molded leadframe strip for encapsulating the at least one semiconductor device. Optionally, a cap is mounted thereby forming a full cavity into the molded leadframe strip for encapsulating the semiconductor device. The cap comprises at least one of the following materials: glass, silicon, ceramic, metal, epoxy, and plastic. In some embodiments, a second leadframe strip is coupled to the first leadframe strip to form a dual leadframe strip. The first leadframe strip and the second leadframe strip are able to be coupled by a soft metal which comprises at least one of the following materials: gold, silver, lead, and tin. The first and second mold compounds can be identical or differing materials.

In another aspect of the invention, an apparatus for forming a land grid array package comprises means for at least partially encasing a first leadframe strip in a first mold compound thereby forming a molded leadframe strip, means for mounting at least one semiconductor device on the molded leadframe strip, means for mounting bondwires on the at least one semiconductor device to effectuate electrical contact between the at least one semiconductor device and the molded leadframe, means for at least partially encasing the molded leadframe strip, the at least one semiconductor device, and bondwires in a second mold compound, and means for singulating the molded leadframe strip to form discrete land grid array packages. In some embodiments, the apparatus further comprises an embossing surface for forming a step cavity into the molded leadframe strip for encapsulating the at least one semiconductor device. Optionally, the apparatus further comprises means for mounting a cap thereby forming a full cavity into the molded leadframe strip for encapsulating the at least one semiconductor device. The cap comprises at least one of the following materials: glass, silicon, ceramic, metal, epoxy, and plastic. In some embodiments, the apparatus comprises means to couple the first leadframe to a second leadframe by a soft metal. The soft metal comprises at least one of the following materials: gold, silver, lead, and tin. The first and second mold compounds can be identical or differing materials.

In another aspect of the invention, a land grid array package comprises a first leadframe, a substrate for supporting the first leadframe, at least one semiconductor die mounted on the first leadframe, a plurality of bondwires to effectuate electrical contact between the at least one leadframe and the at least one semiconductor die. In some embodiments, the substrate comprises a first mold compound. Furthermore, the semiconductor device can comprise a second mold compound for at least partially encasing the at least one leadframe, the substrate, the at least one semiconductor device and the plurality of wirebonds. In some embodiments, the package further comprises a step cavity. Alternatively, the package comprises a cap for forming a full cavity. Optionally, package comprises a second leadframe coupled to the first leadframe by a soft metal. The soft metal is comprised of at least one of the following materials: gold, silver, lead and tin.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features of the invention are set forth in the appended claims. However, for purpose of explanation, several embodiments of the invention are set forth in the following figures.

FIG. **1** is a prior art Chip Scale Package.

FIG. **2** is a prior art Ball Grid Array package in cross section.

FIG. **3** is a process for forming a molded leadframe per an embodiment of the current invention.

FIG. **4**A is a process for forming a molded leadframe per an embodiment of the current invention.

FIG. **4**B is a process for forming a molded leadframe per an embodiment of the current invention.

FIG. **4**C illustrates two exemplary processes for forming a molded leadframe of the current invention.

FIG. **5** is a process for forming individual packages per an embodiment of the current invention.

FIG. **6**A is a semiconductor package per an embodiment of the current invention.

FIG. **6**B is apparatus for realizing the package depicted in FIG. **6**A.

FIG. **6**C is an alternate process for forming a package in FIG. **6**A.

FIG. **6**D is the remainder of the process for forming the package FIG. **6**A.

FIG. **6**E is an alternate apparatus for realizing the package depicted in FIG. **6**A.

FIG. **7** is a process for forming a Land Grid Array (LGA) package.

FIG. **8** is a process for forming a Step Cavity LGA package.

FIG. **9** is a process for forming a Cavity LGA package.

FIG. **10** is a process for forming a Dual Leadframe LGA package.

DETAILED DESCRIPTION

In the following description, numerous details and alternatives are set forth for purpose of explanation. However, one of ordinary skill in the art will realize that the invention can be practiced without the use of these specific details. In other instances, well-known structures and devices are shown in block diagram form in order not to obscure the description of the invention with unnecessary detail. For example, it is commonly known in the art of semiconductor device assembly that assembly is generally done on a matrix array of leadframes, often referred to as leadframe strips, each strip having a plurality of individual positions that will be processed in various ways to form individual packaged semiconductor devices. A position can have one or more semiconductor die within.

In a first aspect of the invention, a process **300** for forming semiconductor packages is detailed in FIG. **3**. A leadframe strip **301** is shown in cross section. In some embodiments, a top mold **302** and a bottom mold **303** are placed to effectuate the injection therein of a mold compound **304**. The top and bottom molds **302**, **303** can be metal, ceramic, or any material having an appropriate thermal characteristic to withstand the temperatures of the mold compound **304** in its liquid state. It is commonly known by those of ordinary skill in the art of semiconductor device manufacturing that a wide variety of mold compounds **304** are able to be used, each having advantages, disadvantages, and characteristics appropriate for a given application. By way of example, in high temperature applications such as microprocessors which generate a significant amount of heat, a high thermal conductivity mold compound **304** is able to be used. What is formed is a molded lead frame **305**. Advantageously, the molded leadframe strip **305** will display enhanced rigidity and robust reliability characteristics. The use of a mold compound **304** further enhances encapsulation and protection from external moisture that standard PCB substrates such as polyimide or FR4 cannot provide.

For more predictable molding results, carrier tape is able to be used effectuate the molding process as shown in FIG. **4**A. A process **400** includes applying tape **405** on its adhesive side to a leadframe strip **401**. The leadframe strip **401** is then placed in a top mold **412** by the top surface of the leadframe **401**. On the opposite side of the leadframe strip **401**, non-adhesive tape **406** is prepared in a tape loader **407** at the bottom mold **413**. Once the leadframe strip **401** is in place between the top mold **412** and the bottom bold **413**, mold compound **404** is injected and fills all empty cavities. When removed from the mold, a molded leadframe strip **410** is formed. Optionally, a de-gate/de-runner step removes excess mold compound **411**.

FIG. **4**B shows an alternate embodiments for the process detailed in FIG. **4**A. In some embodiments, the leadframe strip **401** is able to be placed between the top mold **412** and bottom mold **413** with adhesive tape **405** applied to the bottom. FIG. **4**C shows embodiments wherein the leadframe strip **401** is able to be placed between the top mold **412** and bottom mold **413** without the use of adhesive tape. In an exemplary embodiment, non adhesive tape **406** is able to be provided by a tape loader **407** on the bottom surface of the leadframe strip **401**. In another exemplary embodiment, two tape loaders **407** are provided to effectuate the molding of the leadframe strip **401**. It will be appreciated by those of ordinary skill in the art of semiconductor manufacturing that several embodiments exist to place a leadframe strip **401** between a top mold **412** and a bottom mold **413** and the embodiments discussed herein are written solely to be exemplary and non limiting.

FIG. **5** shows a process **500** for the completion of the semiconductor packaging process. Semiconductor devices **501** are mounted on the molded leadframe strip **502**. In some embodiments, multiple semiconductor devices **501** are mounted in each individual position on the molded leadframe strip **502**. Such devices are known as multi chip modules (MCM). Bondwires **503** are mounted on the semiconductor devices **501** to effectuate electrical contact between the molded leadframe strip **502** and the semiconductor devices **501**. In some embodiments where multiple semiconductor devices **501** are placed in each position, bondwires **503** can be placed to effectuate electrical contact between them as applications require. Next, a second mold compound **505** is applied to the molded leadframe strip **502**. The second mold **505** encases the semiconductor devices **501** and bondwires **503** to protect them from harsh outer environments. In some embodiments, the second mold compound **505** and the first mold compound described in FIGS. **3**, **4**A, **4**B and **4**C are the same. Alternatively, the first and second mold compound **505** are able to be different to meet the demands of particular applications. By way of example, the semiconductor device **501** and the leadframe **401** in FIGS. **4**A, **4**B and **4**C can have different coefficients of expansion in response to heat, and different mold compounds having different thermal characteristics such as thermal resistivity and thermal expansion are able to offset such effects. The molded leadframe strip **502** are then singulated by saw blades **515** to form singulated semiconductor packages **520**, **530** and **540**. The singulated devices **520**, **530** and **540** are generally tested, subjected to stress, and tested again to ensure reliability and to filter out non passing or non standard units.

In some applications, it is advantageous for greater height clearance within the semiconductor package. FIG. **6**A shows a singulated semiconductor package **600** in cross section. Within the package, a step cavity **601** is capable of receiving a thicker semiconductor die **602**, larger bondwires **603** or in certain embodiments multiple stacked die. FIG. **6**B shows an exemplary surface **610** of the mold **412** or **413** shown in FIG. **4**B. Elevated protrusions **611** are placed to coincide with a leadframe strip to emboss a recessed area **601** into the leadframe. In an exemplary embodiment, adhesive tape **621** is applied to the back surface of the leadframe strip **622** as shown in FIG. **6**C. The leadframe is flipped over such that its top surface is embossed by the surface **610** of the mold **412** or **413** having the protrusions **611**.

FIG. **6**D shows the leadframe strip **622** with a first mold compound **623** to form a molded leadframe **630** having recessed areas **601**. To form singulated packages, semiconductor devices **602** and bondwires **603** are affixed onto the molded leadframe **630**. The devices **602**, bondwires **603** and molded leadframe **630** are encased in a second mold compound **650**. The second mold compound **650** and the first mold compound **623** are able to be the same compound or different compounds depending on the application. Saw blades **655** then singulate the molded leadframe strip **630** into individual semiconductor packages **690**.

An alternative surface is shown in FIG. **6**E. In certain applications, such as high temperature applications, thick leadframes are advantageous. To accommodate thick leadframes, the non adhesive tape **610** provided by a tape loader is able to have pre-formed holes **660** configured to receive protrusions **670** on a mold surface **675**. The mold surface **675** can be the surface of the top mold **412** or the bottom mold **413** as shown on FIGS. **4**A, **4**B and **4**C. The mold is able to be formed of metal, ceramic, hard impact rubber, or any other suitable material.

FIG. **7** details a process **700** for forming singulated Land Grid Array (LGA) packaged devices **790**. A leadframe strip **701** is mounted to adhesive tape **702**. In some embodiments, the leadframe strip **701** is a half etched leadframe. The leadframe strip **701** is molded by a first mold compound **703** by any of the processes detailed in FIGS. **4**A, **4**B, **4**C and **5**. The tape **702** is removed forming a molded leadframe strip **705**. Next, semiconductor devices **706** are affixed onto the molded leadframe strip onto each individual position. In some embodiments, multiple devices **706** can be placed in each position as applications require. Bondwires **707** are affixed to effectuate electrical contact between the molded leadframe strip **705** and the devices **706**. The molded leadframe strip **705**, devices **706** and bondwires **707** are encased in a second mold compound **710**. The second **710** and the first **703** are able to be identical mold compounds or different mold compounds as applications require. The double molded leadframe strip **705** is singulated by saw blades **712** forming individual LGA package devices **790**. These individual devices are then able to be tested, marked and bulk packaged for shipping and assembly. It will be apparent to those of ordinary skill in the art of semiconductor device assembly that although few leads **720** are shown, many dozens to hundreds of leads are able to be realized using the process described herein.

In another aspect of the invention, a step cavity LGA and a process for producing the same **800** are disclosed in FIG. **8**. A leadframe strip **801** is mounted to adhesive tape **802**. In some embodiments, the leadframe **801** is a half etched leadframe. The leadframe strip **801** is molded with a first mold compound **803**. By way of example, the first mold compound is able to be a thermoset compound or a thermoplastic compound. Preferably, step cavities **804** are formed by the embossing procedure described in FIGS. **6**A-**6**D. The adhesive tape **802** is removed forming a molded step cavity leadframe strip **805**. At least one semiconductor device **806** is mounted within each cavity **804**. Wirebonds **807** effectuate electrical contact between the semiconductor device and molded step cavity leadframe strip **805**. In some embodiments where multiple semiconductor devices **806** are mounted in each step cavity **804**, wirebonds **807** are able to effectuate electrical contact between the multiple devices **806** as applications require. A second mold compound **810** is formed over the molded step cavity leadframe strip **805**, semiconductor devices **806** and wirebonds **807**. The second mold compound **810** is able to be identical to or different from the first mold compound **803** as applications require. Saw blades **815** singulate the molded step cavity leadframe strip

805 into individual step cavity LGA packaged devices **820**. The devices **820** are then able to be marked, tested and shipped to customers.

In another aspect of the invention, a cavity LGA and a process for making the same **900** are disclosed. A leadframe strip **901** is mounted to adhesive tape **902**. In some embodiments, the leadframe **901** is a half etched leadframe. The leadframe strip **901** is molded with a first mold compound **903**. By way of example, the first mold compound is able to be a thermoset compound or a thermoplastic compound. In some embodiments, step cavities **904** are formed by the embossing procedure described in FIGS. **6**A-**6**E. The adhesive tape **902** is removed forming a molded step cavity leadframe strip **905**. At least one semiconductor device **906** is mounted within each cavity **904**. Wirebonds **907** effectuate electrical contact between the semiconductor device and molded step cavity leadframe strip **905**. In some embodiments where multiple semiconductor devices **906** are mounted in each step cavity **904**, wirebonds **907** are able to effectuate electrical contact between the multiple devices **906** as applications require. A cap **908** is affixed to the molded cavity leadframe strip forming a full cavity **909**. The cap **908** is able to be comprised of silicon, glass, metal, ceramic, or any other convenient material or combination of materials as particular applications require. A second mold compound **910** is formed over the molded step cavity leadframe strip **905**, semiconductor devices **906** and wirebonds **907**. The second mold compound **910** is able to be identical to or different from the first mold compound **903** as applications require. Saw blades **915** singulate the molded step cavity leadframe strip **905** into individual cavity LGA packaged devices **920**. The devices **920** are then able to be marked, tested and shipped to customers.

In some applications, multiple hundreds of I/O are required, and more than one leadframe is required to effectuate contact between a semiconductor device and its application. Furthermore, flexibility in routing I/O is advantageous, since end users can have specific demands as to the locations of I/O on a package landing pattern. To those ends, a dual molded leadframe LGA package and a process for making the same **1000** are disclosed in FIGS. **10**A and **10**B. Referring first to FIG. **10**A, a first leadframe strip **1001** and a second leadframe strip **1002** are coupled to each other. In some embodiments, the first **1001** and second **1002** leadframe strips are held by adhesive tape **1003**. The two leadframe strips are clamped together to effectuate adhesion between them in preparation for a later molding step. In some embodiments, a soft metal **1004** is able to be used to enhance electrical contact between the two leadframe strips. The soft metal **1004** is able to be applied to the top leadframe **1001** or the bottom leadframe **1002**. Referring to FIG. **10**B, the top leadframe **1001** and bottom leadframe **1002** are molded with a first mold compound **1005**. The tape is removed forming a stacked molded leadframe strip **1006**. Semiconductor devices **1010** are mounted and bondwires **1020** effectuate electrical contact between the semiconductor devices **1010** and the stacked molded leadframe strip **1006**. At least one semiconductor device **1010** is mounted in every position and electrically coupled to the stacked molded leadframe strip **1006** via bondwires **1020**. A second mold compound **1030** encases the stacked molded leadframe strip **1006**, semiconductor devices **1010** and bondwires **1020**. The second mold **1030** is able to be identical to or different than the first mold compound **1005**. Saw blades **1035** singulate the stacked molded leadframe strip **1006** forming discrete semiconductor devices **1050**.

While the invention has been described with reference to numerous specific details, one of ordinary skill in the art will recognize that the invention can be embodied in other specific forms without departing from the spirit of the invention. Thus, one of ordinary skill in the art will understand that the invention is not to be limited by the foregoing illustrative details, but rather is to be defined by the appended claims.

We claim:

1. A process of forming semiconductor packages, the process comprising:

a. at least partially encasing a first leadframe strip in a first mold compound thereby forming a molded leadframe strip, wherein the molded leadframe strip includes a first planar surface and a second planar surface that is lower than the first planar surface, wherein at least partially encasing a first leadframe strip in a first mold compound comprises:
   i. placing the first leadframe strip in a mold cavity, wherein the mold cavity includes an emboss feature and is defined by a top mold and a bottom mold, wherein the bottom mold includes a tape loader providing a tape that includes pre-formed holes configured to receive protrusions on a mold surface; and
   ii. injecting the first mold compound into the mold cavity;
b. directly mounting at least one semiconductor device on the first mold compound between a first portion of the second planar surface and a second portion of the second planar surface;
c. mounting bondwires on the at least one semiconductor device to effectuate electrical contact between the at least one semiconductor device and the second planar surface;
d. mounting at least one cap on the molded leadframe strip, wherein each of the at least one cap includes a lateral surface that is perpendicular and is affixed to the first planar surface;
e. at least partially encasing the molded leadframe strip and at least a top portion of the at least one cap in a second mold compound; and
f. singulating the molded leadframe strip to form discrete semiconductor packages.

2. The process of claim **1**, wherein mounting the at least one cap forms a full cavity into the molded leadframe strip for encapsulating the at least one semiconductor device.

3. The process of claim **2**, further wherein the at least one cap comprises at least one of the following materials: glass, silicon, ceramic, metal, epoxy, and plastic.

4. The process of claim **1**, further comprising a second leadframe strip, thereby forming a dual leadframe strip.

5. The process of claim **4**, wherein the first leadframe strip and the second leadframe strip are coupled by a soft metal which comprises at least one of the following materials: gold, silver, lead, and tin.

6. The process of claim **1**, wherein the first and second mold compounds comprise differing material.

7. The process of claim **1**, wherein the first mold compound is a high thermal conductivity mold compound.

8. The process of claim **1**, wherein the first leadframe strip is a half-etched leadframe.

9. The process of claim **1**, wherein one or more semiconductor devices can be placed in an individual semiconductor position on the molded leadframe strip.

10. The process of claim **1**, wherein each of the at least one cavity corresponds to one of the protrusions.

11. A process of forming semiconductor packages, the process comprising:

a. at least partially encasing a first leadframe strip in a first mold compound thereby forming a molded leadframe strip, wherein the first leadframe strip includes at a front surface, a back surface, least one step cavity, a first planar surface and a second planar surface, wherein the first mold compound is in the at least one step cavity, wherein at least partially encasing a first leadframe strip in a first mold compound comprises:

1. placing the first leadframe strip in a mold cavity, wherein the mold cavity includes an emboss feature and is defined by a top mold and a bottom mold, wherein the bottom mold includes a tape loader providing a tape that includes pre-formed holes configured to receive protrusions on a mold surface; and
2. injecting the first mold compound into the mold cavity;

b. directly mounting at least one semiconductor device on the first mold compound that is in the at least one step cavity;

c. mounting bondwires on the at least one semiconductor device to effectuate electrical contact between the at least one semiconductor device and the second planar surface;

d. mounting at least one cap on the molded leadframe strip, wherein each of the at least one cap includes a well on an underside of the at least one cap, wherein a wall defining the well is affixed to the first planar surface;

e. at least partially encasing the molded leadframe strip and at least a top portion of the at least one cap in a second mold compound; and

f. singulating the molded leadframe strip to form discrete semiconductor packages.

12. The process of claim **11**, wherein placing the first leadframe strip in a mold cavity comprises applying adhesive tape to the back surface of the first leadframe.

13. The process of claim **11**, wherein each of the at least one cavity corresponds to one of the protrusions.

14. The process of claim **11**, wherein a full cavity is defined at least by the well, the first mold compound and the second planar surface.

15. The process of claim **11**, wherein the perimeter at a top of the at least one cap is the same size as the perimeter at a bottom of the cap.

16. A process for forming a semiconductor package for applications, the process comprising:

a. at least partially encasing a first leadframe strip in a first mold compound thereby forming a molded leadframe strip, wherein the molded leadframe strip includes at least one step cavity, wherein at least partially encasing a first leadframe strip in a first mold compound comprises:

1. placing the first leadframe strip in a mold cavity, wherein the mold cavity includes an emboss feature and is defined by a top mold and a bottom mold, wherein the bottom mold includes a tape loader providing a tape that includes pre-formed holes configured to receive protrusions on a mold surface; and
2. injecting the first mold compound into the mold cavity;

b. directly mounting at least one semiconductor device on a portion of the first mold compound in the at least one step cavity such that the at least one semiconductor device physically contacts the portion of the first mold compound;

c. mounting bondwires on the at least one semiconductor device to effectuate electrical contact between the at least one semiconductor device and the molded leadframe strip;

d. mounting at least one cap on the molded leadframe strip, wherein each of the at least one cap includes a well on an underside of the at least one cap;

e. at least partially encasing the molded leadframe strip and at least a top portion of the at least one cap in a second mold compound; and

f. singulating the molded leadframe strip to form discrete packages.

17. The process of claim **16**, wherein each of the at least one cavity corresponds to one of the protrusions.

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